AD-A161 927 FUNCTIONAL TESTING OF LSI/VLSI BASED SYSTEMS WITH MEASURE OF FAULT COVERAGE(U) STATE UNIV OF NEW YORK AT ALBANY RESEARCH FOUNDATION S Y SU 05 NOV 82 1/1

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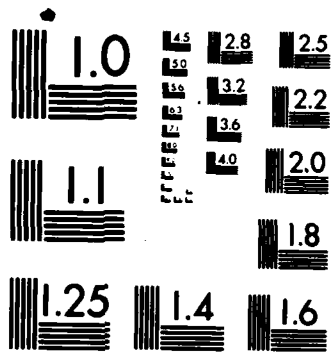

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

SCIENTIFIC AND TECHNICAL REPORT

SECOND QUARTERLY STATUS REPORT

prepared by

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A. Contractor's name and address:

The Research Foundation of
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B. Contract No. DAAB07-82-K-J05-6

C. Date of Report - November 5, 1982

D. Title: The Second Quarterly Report for the project "Functional Testing of LSI/VLSI Based Systems with Measure of Fault Coverage"

E. Period Covered: July 28 to October 27, 1982

F. Description of Progress:

The author has ~~We have~~ studied thoroughly the fundamental contributions made by Thatte and Abraham. The results of our study are reported below.

Thatte and Abraham [1,2] have considered the problem of micro-processor testing. Based on the architectural information available to a user and the instruction set for a given microprocessor, they define a graph model of the microprocessor under consideration. This model is then used to derive necessary tests. Their approach is, first to label the nodes and edges in the graph based on the observability of such nodes and edges. The faults are divided into five different classes namely register decoding, instruction decoding/control, data path, data storage and data manipulation faults.

Explicit models are given for all these fault classes and functional units. It is assumed that no more than one functional unit is faulty, though any number of faults of one class can be present. Procedures are then developed to detect faults of different classes. They have also studied the fault coverage of their tests for a Hewlett Packard system.

References 1 and 2 address the testing of microprocessors at functional level, however, the model and procedures developed by Thatte and Abraham [1,2] have the following major limitations -

(i) Graph Modeling: Though the nodes of a graph are well defined the links definition is largely deductive. It is assumed that a user can deduce the micro-sequencing of the execution of an instruction from the knowledge of the instruction. Though this appears to be a natural limitation in user environment, yet it gives rise to a problem "If for a single instruction two different micro-sequences can be deduced, can choice of either one of them results into an effective test or both such sequences need to be considered to have an effective fault coverage?"

(ii) Fault Modeling: One of the limitations has already been pointed out i.e. only one class of faults is assumed to be present. In addition, faults in instruction decoding/control function are much too restrictive. Faults in timing unit which can increase the execution time or cause a partial execution of an instruction are explicitly left out. Another limitation of the method is that it can not be used for design varification purposes for the following reason: It is assumed that if due to a fault an instruction I_j becomes I_k, then no fault can cause I_p to become I_j. Though this will hold in most physical fault conditions yet this assumption does not hold for design faults.

Furthermore, no fault model is presented for faults in data manipulation unit. It is assumed that the tests are available to test ALU in the microprocessor.

(iii) Test Derivation: Most of the procedures are given for graphs with certain restrictions. Though, this is not a major limitation, we believe that the results can be extended with some effort.

We plan to generalize Thatte and Abraham's work by looking into the removal of the above three limitations.

In addition to the above Lai [3] has considered the problem of functional testing of digital systems. He defines a graph of digital system using a new graph description language and tests are generated from the graph so described. One of the major limitations of that work is loss of timing information. Unlike Thatte and Abraham [1] the test method is used to generate bit strings and not test programmes. Also, we believe Lai's [3] graph description language is not well suited to bus oriented systems like microprocessors. Thus the major limitation of Lai's [3] work is its inability to handle faults in timing/timing unit and unsuitability to generate test programs.

Given the functions of an integrated circuit chip, without the knowledge of its imlementation, we found a systematic way to detect and locate the following five types of faults in the input and output pins of the integrated ciricuit chip [4].

1) bridging (short circuit) faults among input lines
2) bridging faults among output lines
3) feedback bridging faults between inputs and outputs
4) stuck-at faults at inputs
5) stuck-at faults at outputs

Our approach is to use an array of special test patterns such that the output responses are distinct. In our paper [4]′, we show how the above five types of faults in a RAM and an ALU (Texas Instruments circuit types SN 54181 and SN74181) can be tested. The generated patterns are verified by a digital computer to ensure the completeness of the test set. See the attached manuscript for detail.

[1] S.M. Thatte and J.A. Abraham, "Test Generation for Microprocessors" IEEE Transaction on Computers, Vol C-29, No. 6, June 1980, pp. 429-441.

[2] S.M. Thatte, "Test Generation For Microprocessors" Ph.D. Dissertation, Co-ordinated Science Laboratory, University of Illinois at Urbana-Champaign, 1979.

[3] K.W. Lai, "Functional Testing of Digital Systems," Ph.D. Dissertation, Dept. of Computer Science, Carnegie-Mellon University, December 1981.

[4] S. Xu and S.Y.H. Su, "A Systematic Technique for Detecting and Locating Bridging and Stuck-at Faults in LSI/VLSI" to be submitted for publication.

Current quarter actual cost: $7,188.57

Cumulative cost to date: $13,718.91

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